

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-47 (cancelled)

48. (Currently amended) An integrated semiconductor structure comprising:
- a multijunction solar cell including a first photoactive junction formed in a substrate forming a first subcell, and a second photoactive junction formed in a region overlying said substrate forming a second subcell; and
- means integral to a portion of said first subcell for passing current when said multijunction solar cell is shaded, wherein said means and said first subcell have identical sequences of layers with substantially the same thickness.
49. (Previously submitted) The structure as defined in claim 48, wherein said means for passing current is a bypass diode formed on the substrate.
50. (Previously submitted) The structure as defined in claim 49, wherein said first subcell and said bypass diode are formed in the same process.
51. (Previously submitted) The structure as defined in claim 49, wherein the bypass diode has a Schottky junction.
52. (Currently amended) An integrated semiconductor structure comprising:
- a multijunction solar cell including a bottom subcell formed on a substrate; and

means integral to a portion of said bottom subcell for passing current when said multijunction solar cell is shaded, wherein said means and said bottom subcell have identical sequences of layers with substantially the same thickness.

53. (Previously submitted) The structure as defined in claim 52, wherein said bottom subcell is formed on a first portion of the substrate and said means for passing current is a bypass diode formed on a second portion of the substrate that is laterally spaced from said first portion.

54. (Currently amended) The structure as defined in claim [[52]] 53, wherein said ~~first~~ bottom subcell and said bypass diode are formed in the same process.

55. (Currently amended) The structure as defined in claim [[52]] 53, wherein said ~~epitaxially grown bypass~~ diode is electrically connected across the subcells of the multijunction solar cell to protect said subcells against reverse biasing.

56. (Currently amended) The structure as defined in claim [[52]] 53 wherein the bypass diode has a Schottky junction.

57. (Currently amended) An integrated semiconductor structure comprising:
a multijunction solar cell including a first solar cell formed on a substrate; and

a bypass diode integral to a portion of said first solar cell and directly electrically connected to the base of said first solar cell for passing current when said multijunction solar cell is shaded, wherein said bypass diode and said first solar cell have identical sequences of layers with substantially the same thickness; and further wherein said first solar cell is the bottom solar cell.

58. (Currently amended) The structure as defined in claim [[56]] 57, wherein said first solar cell is formed on a first portion of the substrate and said bypass diode is formed on a second portion of the substrate spaced apart from said first portion.

59. (Currently amended) The structure as defined in claim [[56]] 57, further comprising a metal layer connecting said bypass diode to the base of the first solar cell.

60. (Previously submitted) An integrated semiconductor structure comprising:
a multijunction solar cell including first and second solar cells on a substrate;
means integral to a portion of said first solar cell for passing current when said multijunction solar cell is shaded; and
a planar metal layer connecting said multijunction solar cell and said means for passing current, wherein
one end of said metal layer is coupled to the base of said first solar cell and
another end of said metal layer is coupled to one terminal of said means for passing current;
and further wherein

said means for passing current and said first solar cell have identical sequences of layers with substantially the same thickness.

61. (Currently amended) The structure as structure as defined in claim ~~[[59]]~~ 60, wherein said first solar cell is formed on a first portion of the substrate, and said means for passing current is a bypass diode formed on a second portion of the substrate.

62. (Currently amended) The structure as defined in claim 60, wherein ~~said first portion and said second portion~~ multijunction solar cell and said means for passing current are separated by a trough, and said metal layer lies over said trough.

63. (Currently amended) The structure as defined in claim ~~[[59]]~~ 60, wherein both said first solar cell ~~grown~~ and said bypass diode are formed in the same process.

64. (Currently amended) The structure as defined in claim 62, wherein ~~said epitaxially grown diode~~ means for passing current is electrically connected across at least said first and second cells to protect said first and second cells against reverse biasing.

65. (Currently amended) A solar cell semiconductor device comprising:
an integral semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms the first cell of a multijunction solar cell; and

a second region laterally spaced apart from said first region and in which the sequence of layers corresponding to the sequence of layers forming said first cell forms a bypass diode to protect said multijunction solar cell against reverse biasing, wherein the first region and the second region have identical sequences of layers with substantially the same thickness.

66. (Previously submitted) A device as defined in claim 65, wherein the sequence of layers of said first cell and the sequence of layers of the bypass diode are formed in the same process step.

67. (Previously submitted) A device as defined in claim 65, wherein the semiconductor body includes a Ge substrate, and at least one of the cells is fabricated at least in part with GaAs.

68. (Previously submitted) A solar cell semiconductor device comprising:
a substrate;
a sequence of layers of material deposited on said substrate, including a first region in which the sequence of layers of material forms at least one cell of a multijunction solar cell, and a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing, wherein the first region and the second region have identical sequences of layers with substantially the same thickness; and

a discontinuous lateral conduction layer deposited on said substrate for making electrical contact to an active region of said bypass diode.

69. (Previously submitted) A device as defined in claim 68, wherein said lateral conduction layer in the first region is physically separated from the lateral conduction layer in the second region.

70. (Previously submitted) A device as defined in claim 68, wherein said lateral conduction layer is a highly doped layer.

71. (Previously submitted) A device as defined in claim 70, wherein said lateral conduction layer is composed of GaAs.

72. (Previously submitted) A device as defined in claim 68, wherein one of the layers of said sequence of layers is an etch stop layer, and said lateral conduction is disposed directly over said etch stop layer.

73. (Previously submitted) A device as defined in claim 68, wherein said substrate includes a photoactive junction.

74. (Previously submitted) A device as defined in claim 73, wherein said substrate is germanium.

75. (Previously submitted) A device as defined in claim 73, wherein said substrate forms an electrical connection path between said multijunction solar cell as said bypass diode.

76. (Previously submitted) A device as defined in claim 68, further comprising:
a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to (i) electrically short layers of said second region, and (ii) connect the substrate to said lateral conduction layer to complete the electrical circuit between the multijunction solar cell and the bypass diode.

77. (Currently amended) A solar cell semiconductor device comprising:
a substrate;
a sequence of layers of semiconductor material deposited on said substrate including a first region in which the sequence of layers of semiconductor material forms at ~~least~~ least one cell of a multijunction solar cell, and a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing, wherein the first region and the second region have identical sequences of layers with substantially the same thickness; and
a lateral conduction layer deposited on said substrate including a first portion disposed in said first region, and a second portion disposed in said second region and physically separated from said first portion.

78. (Previously submitted) A device as defined in claim 77, wherein said lateral conduction layer is a highly doped layer.

79. (Previously submitted) A device as defined in claim 77, wherein said lateral conduction layer is composed of GaAs.

80. (Previously submitted) A device as defined in claim 77, wherein one of the layers of said sequence of layers is an etch stop layer, and said lateral conduction layer is disposed directly over said etch stop layer.

81. (Previously submitted) A device as defined in claim 77, wherein said second portion of said lateral conduction layer makes electrical contact with a first InGaP layer of said bypass diode.

82. (Previously submitted) A device as defined in claim 81, wherein said bypass diode further comprises a GaAs layer disposed over said first InGaP layer, and a second InGaP layer disposed over said GaAs layer.

83. (Previously submitted) A device as defined in claim 82, further comprising a metal layer deposited over said second InGaP layer and forming a Schottky junction with said second InGaP layer.

84. (Previously submitted) A device as defined in claim 77, wherein said substrate includes a photoactive junction.

85. (Previously submitted) A device as defined in claim 77 wherein said substrate is germanium.

86. (Previously submitted) A device as defined in claim 77, wherein said substrate forms an electrical connection path between said multijunction solar cell as said bypass diode.

87. (Previously submitted) A device as defined in claim 86, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

88. (Previously submitted) A solar cell semiconductor device comprising:
a substrate;
a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and
a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing, wherein the first region and the second region have identical sequences of layers with substantially the same thickness; and

a highly conductive lateral conduction layer deposited on said substrate for making electrical contact with one layer of said bypass diode and forming a contact region to allow said bypass diode to be electrically connected to said multijunction solar cell.

89. (Previously submitted) A device as defined in claim 88, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

90. (Previously submitted) A device as defined in claim 88, wherein said lateral conduction layer includes a first portion disposed in said first region, and a second portion disposed in said second region and separated from the first portion.

91. (Previously submitted) A device as defined in claim 88, wherein said lateral conduction layer is a highly doped layer composed of GaAs.

92. (Previously submitted) A device as defined in claim 90, wherein said second portion of said lateral conduction layer makes electrical contact with a first active layer of said bypass diode.

93. (Currently amended) A solar cell semiconductor device comprising:
a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and

a second region laterally spaced apart from said first region, wherein said second region and said first region have identical sequences of layers with substantially the same thickness; and

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting the layers of said second region to enable a bypass diode to be formed in said second region.

94. (Previously submitted) A device as defined in claim 93,

wherein said metal layer connects said multijunction solar cell and said bypass diode with one end of said metal layer being coupled to the base of said one solar cell and another end of said metal layer is coupled to one terminal of said bypass diode.

95. (Previously submitted) A device as defined in claim 93, wherein said first portion and said second portion are separated by a trough, and said metal layer lies over at least a portion of said trough.

96. (Currently amended) A device as defined in claim 93, wherein at least one layer of said first solar cell and said bypass diode are ~~substantially~~ simultaneously formed in the same process.

97. (Previously submitted) A device as defined in claim 93, wherein said bypass diode is electrically connected by said metal layer across said solar cell to protect said solar cell against reverse biasing.

98. (Previously submitted) A device as defined in claim 93 further comprising a lateral conduction layer deposited on said substrate for electrically connecting the multijunction solar cell to said bypass diode.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.